SR1020 Datasheet

SPARK Microsystems

PRELIMINARY

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Abstract

This document details the preliminary datasheet for the SR1020 engineering sample. The performance figures are only valid for the engineering sample and only indicative of the performance of the production version.

Contents

1 Device Overview

1.1 Description

The SR1020 is a digitally programmable UWB wireless transceiver. It transmits in the license-free UWB spectrum from 6.0 - 9.3 GHz by using short impulses that enable highly robust and energy efficient communications.

The transceiver allows for the dynamic shaping of its output spectrum to comply with international UWB emission limits or tailor its emissions to a wide range of spectral masks. The circuits are aggressively duty cycled to enable ultra low power operation. The ASIC is composed of an impulse radio with an RF transmitter and receiver, power management unit, sleep counter and digital / baseband hardware. The ASIC interfaces via an SPI interface to an MCU running the link layer.

The SR1020 can achieve ultra-low power consumption within a wide range of data rates making it a highly versatile solution.

It is an excellent solution for wireless applications that benefit from high degrees of energy efficiency, short latency, versatile operation or robust communications.

1.2 Features

- UWB Radio Transceiver
  - 6.0 - 9.3 GHz frequency band
  - 20.48 Mbps symbol rate
  - 500 MHz to 3 GHz reconfigurable TX bandwidth
  - Up to 3 dBm/20MHz tunable TX symbol energy
  - -75 dBm/20MHz RX sensitivity
  - 100 Ohm differential antenna interface, no matching components required
- Integrated clock management
  - Only one 32.768 kHz external XTAL required
  - Always-on real time clock[1]
  - Synthesized 20.48 MHz system clock
- Ultra-low power consumption
  - 1.8 V - 3.3 V supply voltage
  - Internal DC-DC converter
- Versatile digital core
  - Up to 50 MHz SPI interface
  - Modem supports OOK modulation, differential encoding, 32-bit sync word, punctured FEC, and 16-bit CRC
  - Independent 1 kb TX and 1 kb RX FIFOs
  - 1 kb NVM memory
- Supply current @ 3.3 V
  - 0.39 mA/Mbps Active RX
  - 0.12 mA/Mbps Active TX
  - 250 uA Idle mode (PLL on, DC-DC on)
  - 41 uA Shallow Sleep mode (PLL on, DC-DC off)
  - 920 nA Deep Sleep mode (PLL off, RTC on)
  - 55 nA Shutdown mode (RTC off, no retention)
- 28 pins, 4 mm x 4 mm QFN package for use in compact systems
- Small number of external components required

1.3 Device Information

Table 1: Package Information

PART NUMBER	PACKAGE	BODY SIZE	QUANTITY
SR1020-28QFN	QFN28	4x4mm	1
SR1020-28QFN-TR	QFN28	4x4mm	4000

[1] Except in SHUTDOWN mode.

2 System Overview

2.1 Block Diagram

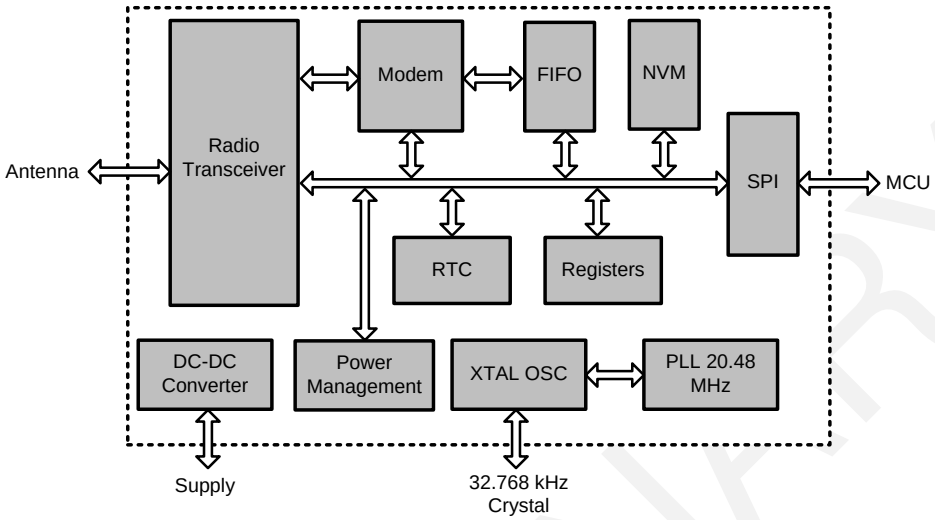


Figure 1: System Block Diagram

2.2 Radio Transceiver, Modem and FIFO

The radio transceiver is a proprietary impulse radio which operates in the license-free UWB spectrum. The radio is powered by the 1.0V power domain and is heavily power cycled to reduce power consumption.

The transmitter is highly flexible and can be adapted to efficiently fill the available RF spectrum, taking into account the realized antenna gains in a specific implementation. The receiver operates in non-coherent mode and is robust to in-band and out-of-band interferers. On-Off Keying (OOK) is supported by the modem, as well as differential encoding, punctured FEC (1.0, 1.33, 1.66 and 2.0 rate), variable preamble length, 32-bit sync word, 8 or 16-bit address, and 16-bit programable CRC. A 1kb RX FIFO and 1kb TX FIFO is available to buffer the packets.

The data rate and available RF spectrum constrain the allowable transmitter parameters. As a result, the link budget is higher for low datarate links and lower for high datarate links.

2.3 Power Modes

There are four different power modes in the SR1020:

- *P0 Active Mode*: All systems are active and reception or transmission is in progress.
- *P1 Idle Mode*: The receiver and transmitter are off and the system is waiting.
- *P2 Shallow Sleep Mode*: The 1V power domain is off, but the bias and PLL domains are powered on.
- *P3 Deep Sleep Mode*: All domains are powered off except the XTAL oscillator and RTC. SPI communication is fully functional.
- *P4 Shutdown Mode*: All domains are powered off and SPI communication is not functional.

Accurate power cycling is key to reaching high energy efficiencies in the SoC. Deeper sleep modes consume less power but take longer to wake up from. Power modes cannot be skipped, for example: waking up from P3 to P0 requires traversing through P2 and P1 first. The sleep controller contains automatic sleep and wakeup conditions

to facilitate this process.

2.4 Reset and Shutdown

At system startup, the RSTN pin should be held low until the supply voltage is stable. Normal operation starts after pulling RSTN high.

The Shutdown mode allows minimum current consumption, and can be entered by pulling SHUTDOWN high. Wakeup from Shutdown mode is accomplished by pulling SHUTDOWN low, while keeping RSTN low to reset the ASIC. Normal operation starts after pulling RSTN high.

2.5 Interrupt Controller and RTC

The interrupt controller can be programmed to launch an asynchronous interrupt on IRQ on certain events. This allows the MCU to sleep. Common interrupt events include packet reception, frame transmit completed, wakeup from sleep, and more.

A low-power Real Time Clock (RTC) is available in every mode except Shutdown, which can wake up into higher sleep modes.

2.6 SPI

The Serial Peripheral Interface (SPI) allows modification of the registers and acts as the interface to the FIFOs. The fundamental operation mode is 8-bit slave. MOSI is sampled on the SCK rising edge, and MISO is setup on the falling edge of SCK. This corresponds to SPI mode 0.

Communication occurs in 2 bytes packets (unless in burst mode), with the first byte being the command byte and the second byte being the data. The command byte contains a 6-bit address in LSBs (bits 5-0), the write flag in bit 6 and the burst flag in bit 7. When the write flag is high, the data byte on MOSI is written to the address. If the write flag is low, the data byte in MISO contains the content of the register. The burst flag supports multi-byte transfers to and from the FIFOs.

The SPI interface is always available, in every sleep mode except Shutdown. The timing characteristics of the SPI interface can be found in Table 15.

2.7 Clocks

A 32.768 kHz clock is generated by the XTAL oscillator using an external crystal. This clock powers the Real Time Clock (RTC) implementation.

A 20.48 MHz clock is synthesized on-chip from the XTAL clock using a PLL. This PLL requires an off-chip loop filter and is power cycled according to the usage profile.

It is also possible to supply an external 32.768 kHz and/or 20.48 MHz clock from elsewhere in the system.

The XTAL_CLK and PLL_CLK pins can be configured as clock inputs for the 32.768 KHz and 20.48 MHz clock respectively. These clocks must conform to the specifications in Table 8, 9, 10, and 11.

Warning: PLL_CLK or XTAL_CLK pins are pulled down to ground at startup. If an external oscillator is connected to one of those pins, and if that oscillator is also used by other devices, then these might be prevented from working normally while the radio is not completely configured.

2.8 Power Management

A buck DC-DC converter generates a 1.0 V regulated supply from the main power supply. This supply is available in Idle and Active mode. The NVM, radio transceiver and modem are powered by this supply.

2.9 NVM

A 1 kb Non Volatile Memory (NVM) is available for storing calibration data.

3 Pinout

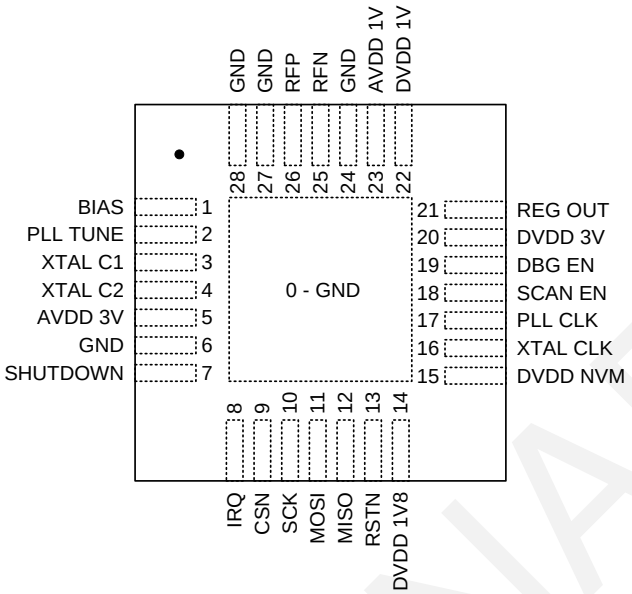


Figure 2: QFN28 package pins (top view through package).

Table 2: Pinout.

Name	Type	Description
Radio Transceiver		
RFP	Analog Input/Output	Positive RF input/output.
RFN	Analog Input/Output	Negative RF input/output.
SPI		
CSN	Digital Input	SPI Chip Select.
SCK	Digital Input	SPI clock.
MOSI	Digital Input	Master-Out-Slave-In.
MISO	Digital Output	Master-In-Slave-Out.
Clock Interface		
XTAL_C1	Analog Input	32.768 kHz crystal oscillator pin 1.
XTAL_C2	Analog Output	32.768 kHz crystal oscillator pin 2.
PLL_TUNE	Analog Input/Output	Connect to PLL loop filter.
Bias Interface		
BIAS	Analog Input/Output	Current reference, connect to +/- 1% 2.2M Ohm resistor.
Power Supply		
AVDD_3V	Power	Supply for analog circuits.
DVDD_3V	Power	Supply for switching/digital circuits.
AVDD_1V	Power	Regulated 1V supply for analog circuits.
DVDD_1V	Power	Regulated 1V supply for switching/digital circuits.
DVDD_1V8	Decouple	Connect to decoupling capacitor.
REG_OUT	Analog Output	Output of DC-DC regulator.

GND	Power	All GND pins must be connected together in the lowest impedance possible. Return currents are directed through the QFN thermal pad.
Miscellaneous		
DVDD_NVM	Power	NVM programming supply, connect to GND.
SHUTDOWN	Digital Input	Normal operation when pin is low, chip is off when pin is high. Connect to GND if not used.
RSTN	Digital Input	Main reset pin; driving it low resets the SoC.
IRQ	Digital Output	Generates user-configurable external interrupt.
DBG_EN	Digital Input	Debug pin, connect to GND.
SCAN_EN	Digital Input	Debug pin, connect to GND.
PLL_CLK	Digital Input/Output	20.48 MHz external clock input/output, leave unconnected if not used.
XTAL_CLK	Digital Input/Output	32.768 kHz external clock input/output, leave unconnected if not used.

4 Application Circuit

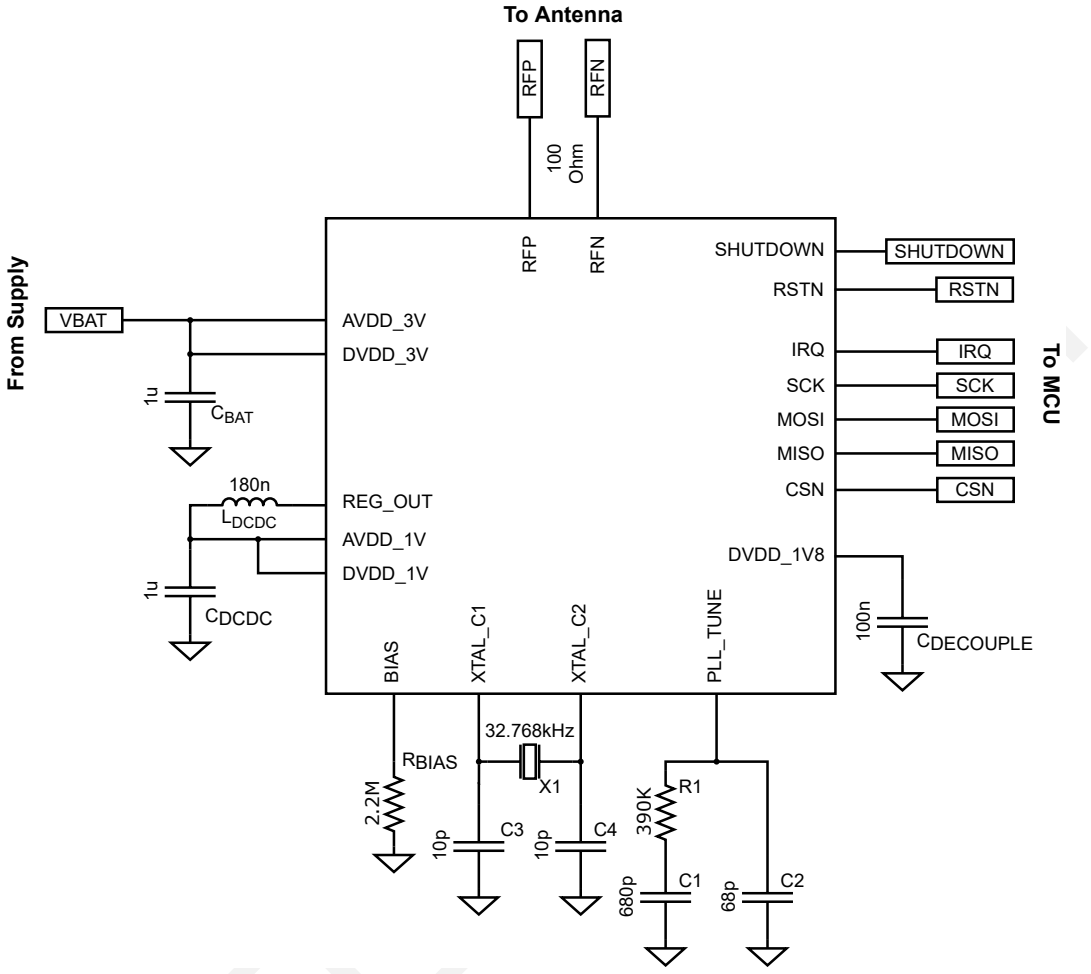


Figure 3: Application circuit.

The schematic of a typical application is given in Fig. 3. Please observe the following guidelines:

- Connect `RFP` and `RFN` to the balun/antenna with a 100 Ohm differential transmission line.
- Connect `AVDD_3V` and `DVDD_3V` to the supply voltage with a low impedance trace.
- Place C_{BAT} as close as possible to `DVDD_3V`. C_{BAT} can be increased for better supply noise rejection.
- Only place a decoupling capacitor on `DVDD_1V8`, this is not a supply pin.
- Connect `CS_N`, `SCK`, `MOSI`, `MISO` and `IRQ` to your MCU. Use of `RSTN` and/or `SHUTDOWN` is optional. If not used, connect `SHUTDOWN` to `GND`, and `RSTN` to an RC network as shown in Figure 4.
- Connect `DEBUG_EN`, `SCAN_EN` and `DVDD_NVM` to `GND`.
- When using `XTAL_CLK` and/or `PLL_CLK` as clock inputs, connect to your clock source. Leave unconnected otherwise.
- **Warning**: `PLL_CLK` and `XTAL CLK` pins are pulled down to ground at startup. If an external oscillator is connected to one of those pins, and if that oscillator is also used by other devices, then these might be prevented from working normally while the radio is not completely configured.
- Minimize the capacitance on the `REG_OUT` node, including the parallel capacitance of the inductor.
- Use a 1% 2.2 MΩ resistor for R_{BIAS}.
- Adjust C3 and C4 to the specifications of your crystal.

- It is advised to use an inductor for L_{DCDC} with $< 1\Omega$ ESR, $>$ 200 mA saturation current, and $>$ 200 MHz self-resonance frequency.
- Connect all GND pads together with low impedance.

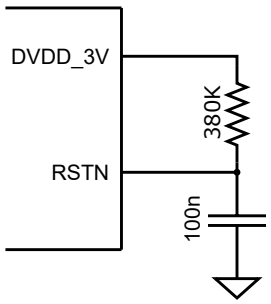


Figure 4: Alternative reset network.

5 Electrical Characteristics

Default measurement conditions: AVDD_3V, DVDD_3V = 2.5 V, temperature = 25 °C.

Table 4: Absolute Maximum Ratings

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Storage temperature		-50	150	°C
Pin voltage (all pins except AVDD_1V, DVDD_1V, DVDD_1V8)		-0.3	3.6	V
Pin voltage (AVDD_1V, DVDD_1V)		-0.3	1.1	V
Pin voltage (DVDD_1V8)		-0.3	1.98	V
ESD (Human Body Model)			2000	V
ESD (Charged Device Model)			500	V

Table 5: Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating temperature		-40		85	°C
Supply voltage[2]	Voltage on AVDD_3V, DVDD_3V	1.8		3.3	V
Supply slew rate[3]	Voltage on AVDD_3V, DVDD_3V			3	mV/us

Table 6: DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown current	3.3 V supply voltage		55		nA
Deep sleep current	3.3 V supply voltage		920		nA
	2.5 V supply voltage		640		nA
	1.8 V supply voltage		570		nA
shallow sleep current	3.3 V supply voltage		41		uA
	2.5 V supply voltage		41		uA
	1.8 V supply voltage		40		uA
Idle current	3.3 V supply voltage		250		uA
	2.5 V supply voltage		270		uA
	1.8 V supply voltage		310		uA
Active RX current	3.3 V supply voltage		8.0		mA
	2.5 V supply voltage		9.2		mA
	1.8 V supply voltage		11.8		mA
Active TX current[4]	3.3 V supply voltage		2.4		mA
	2.5 V supply voltage		2.8		mA
	1.8 V supply voltage		3.5		mA

DC current consumption is reduced by duty cycling depending on data rate, as further outlined in Section 6.4.

[2] Accuracy of AVDD_3V and DVDD_3V should be within +/- 5%.

[3] When a coin cell battery with high internal resistance is used, it is recommended to add a 10 uF capacitor to the AVDD_3V, DVDD_3V net in order to meet this requirement.

[4] 0 dBm/20MHz symbol energy, random data

Table 7: Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset hold time	RSTN low	10			ms
NVM startup time	After entering Idle mode from Shallow Sleep	25			us
Transition time, Shutdown to Deep sleep	Unconnected DVDD_1V8		20		ms
Transition time, Deep sleep to Shallow sleep			3		ms
Transition time, Shallow sleep to Idle			16		us
Transition time, Idle to Active			500		ns

Table 8: Internal XTAL Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal oscillator frequency			32.768		kHz
Load capacitance			10		pF
Crystal frequency tolerance		-100		100	ppm
Startup time			1		s

Table 9: External XTAL Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency			32.768		kHz
Frequency tolerance		-100		100	ppm
Duty cycle		40		60	%
Jitter	Cycle-to-cycle, RMS			2	ns

Table 10: Internal PLL Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup time	PLL filter: C1 = 640 pF, C2 = 64 pF, R1 = 380 kΩ		3		ms
Output frequency			20.48		MHz

Table 11: External PLL Clock Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency			20.48		MHz
Frequency tolerance		-100		100	ppm
Duty cycle		40		60	%
Jitter	N-cycle, N=1000, RMS			2	ns

Table 12: DC-DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage			1.0		V
Efficiency	20 mW load		79		%
Ripple voltage	C_{DCDC} = 1.0 uF, L_{DCDC} = 180 nH		10		mV

Table 13: Radio Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency band		6.0		9.3	GHz
Symbol rate			20.48		Mb/s
Transmitter output power[5]	Max symbol energy		3		dBm/20MHz
	Step		0.5		dB
	Min symbol energy		-12		dBm/20MHz
Receiver sensitivity	Symbol energy		-75		dBm/20MHz
Link budget	0 dBm/20MHz transmitted symbol energy		75		dB
Blocker power[6]	$\leq$ 2.0 GHz		0		dBm
	2.0 to 3.0 GHz		-5		dBm
	3.0 to 4.5 GHz		-20		dBm
	4.5 to 5.5 GHz		-15		dBm
	5.5 to 6.0 GHz[7]	-25		-15	dBm

Table 14: IO Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input low-level voltage				0.35*DVDD_3V	V
Input high-level voltage		0.62*DVDD_3V			V
Output low-level voltage				0.10*DVDD_3V	V
Output high-level voltage		0.90*DVDD_3V			V
Output low-level current				15	mA
Output high-level current				13	mA
Rise time	DVDD_3V = 3.3 V, 10 pF load		2.8		ns
Fall time	DVDD_3V = 3.3 V, 10 pF load		2.1		ns

Table 15: SPI Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCK period		25			ns
SCK duty cycle			50		%
CS_ setup to SCK		12			ns
CS_ hold after SCK		12			ns
MOSI setup to SCK		0.0			ns
MOSI hold after SCK		4.8			ns
MISO delay after SCK	10 pF load	7.0			ns

[5] As expressed in the average power during the symbol time (i.e. the total energy in a symbol).
[6] Interferer power at which sensitivity is reduced by 3 dB.
[7] Depending on the used UWB channel

6 Operational Details

6.1 Power States

The power states are summarized in Table 16.

Table 16: Power States

	SHUTDOWN	DEEP SLEEP	SHALLOW SLEEP	IDLE	ACTIVE
Register retention	No	Yes	Yes	Yes	Yes
SPI communication	Off	On	On	On	On
PLL clock	Off	Off	On	On	On
DC-DC output	Off	Off	Off	On	On
Radio	Off	Off	Off	Off	On
Next state	DEEP SLEEP	SHALLOW SLEEP	IDLE	ACTIVE	Any
Time to next state	20 ms	3 ms	16 us	500 ns	Immediately
Current @ 3.0 V supply voltage	55 nA	750 nA	45 uA	250 uA	2 to 7 mA

6.2 Power-up Sequence

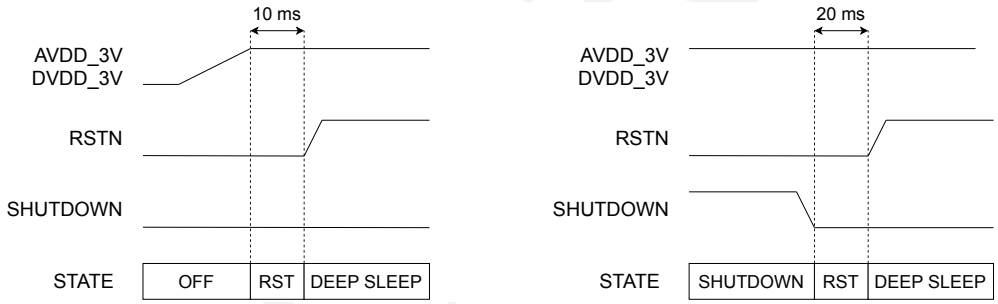


Figure 5: Timing sequence during power on (left) and shutdown (right).

Figure 5 illustrates the power-on sequence and wake-up out of shutdown. Note that in both sequences the digital core is initialized to the default register state.

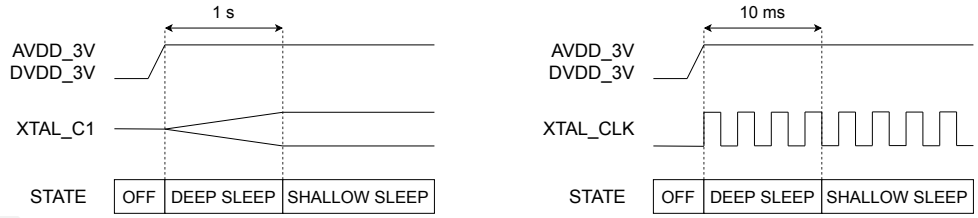


Figure 6: XTAL sequence with internal (left) and external (right) 32.768 KHz source.

After power-on or leaving shutdown mode, the XTAL clock source has to provide a stable 32.768 KHz clock before deep sleep can be exited into shallow sleep. An external 32.768 KHz clock source can be used as an input to the `XTAL_CLK` pin, as shown in Figure 6.

Warning: `PLL_CLK` or `XTAL_CLK` pins are pulled down to ground at startup. If an external oscillator is connected to one of those pins, and if that oscillator is also used by other devices, then these might be prevented from working normally while the radio is not completely configured.

6.3 Sleep Timing

Depending on the packet rate, the radio can transition in either the deep sleep, shallow sleep or idle state in between packets. Figure 7 illustrates the state transistions in these three modes.

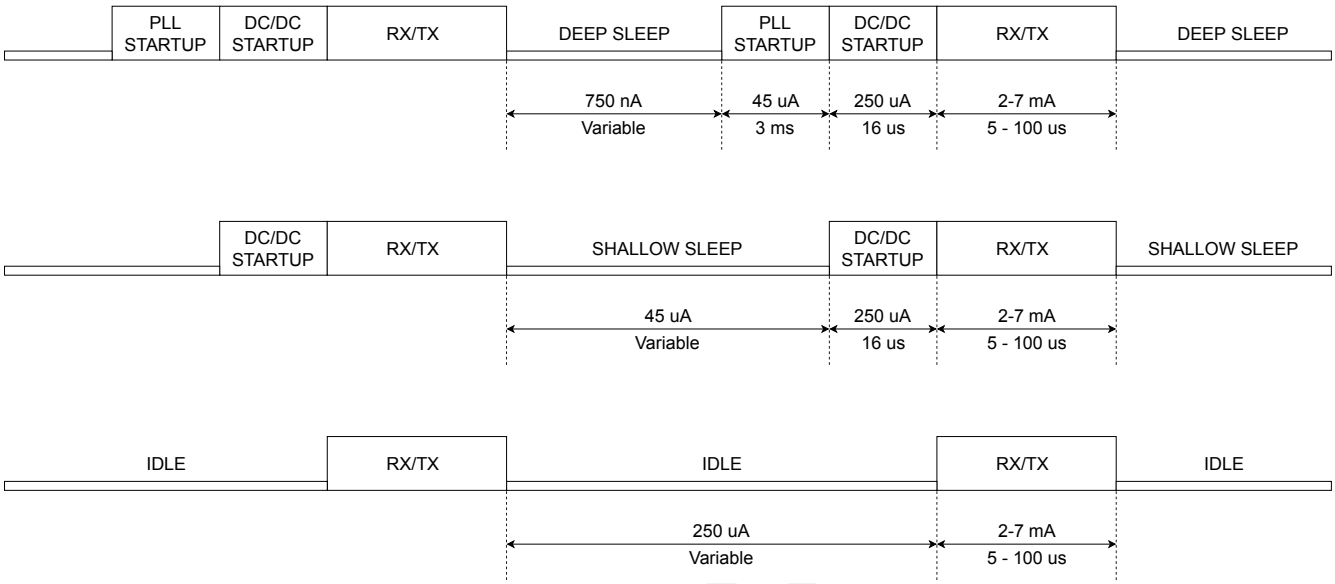


Figure 7: Power profiles (at 3.3 V supply voltage) for deep sleep (top), shallow sleep (middle) and idle (bottom).

Each state draws a different current from the supply, please refer to Table 6. Peak currents in the RX or TX active state can be partially supplied by the supply decoupling capacitor on the `AVDD_3V`, `DVDD_3V` net.

6.4 Power Consumption Model

The following equation captures a first order model for the average power consumption, P_{avg}, of the ASIC:

$$\begin{aligned} P_{avg} &= P_{sleep} + R_{packet} \cdot \left[E_{startup} + E_{bit} \cdot N_{bits} \right] \\ N_{bits} &= N_{guard} + N_{preamble} + N_{payload} \cdot K_{mod} \end{aligned} \tag{1}$$

where P_{sleep} is the sleep power, $E_{startup}$ is the energy required to startup a packet, E_{bit} is the energy to transmit or receive a bit, R_{packet} is the number of packets received/transmitted per second, N_{guard} is the number of symbols in the guard interval in number of symbols (typically 0 for TX and 50 for RX), $N_{preamble}$ is the number of symbols in the preamble (typically 100), and K_{mod} is the modulation / FEC multiplier (which is equal to the FEC rate without, and twice the FEC rate with differential encoding).

This equation has three parts: a constant part due to sleep power, a part that scales with the packet rate R_{packet}, and a part that scales with the data rate $R_{packet} \cdot N_{payload}$.

Table 17 states the coefficients for 1.8, 2.5 and 3.3 V supply voltage.

Table 17: Power coefficients

	Deep Sleep			Shallow Sleep			Idle			Unit
Supply voltage	1.8	2.5	3.3	1.8	2.5	3.3	1.8	2.5	3.3	V
P_{sleep}	1.0	1.6	3.0	72	102	135	558	675	825	uW
$E_{startup}$[8]	513	635	766	8	10	13	0	0	0	nJ/packet
$E_{bit,RX}$	1.0	1.1	1.3	1.0	1.1	1.3	1.0	1.1	1.3	nJ/bit
$E_{bit,TX}$	0.31	0.34	0.39	0.31	0.34	0.39	0.31	0.34	0.39	nJ/bit

The three sleep states offer different trade offs between sleep power, startup energy, and startup time.

Figure 8 gives an example for 64 bytes payload per packet and FEC 1.33.

In this example :

- At a payload data rate under 128kbps , the deep sleep state offers a low sleep current at the cost of an energy cost to startup for a packet.
- Between 128 kbps and 2 Mbps, the shallow sleep state offers medium sleep power at a low startup cost.
- Above 2 Mbps, the startup time from shallow sleep can become disadvantageous, and the idle state can be used.

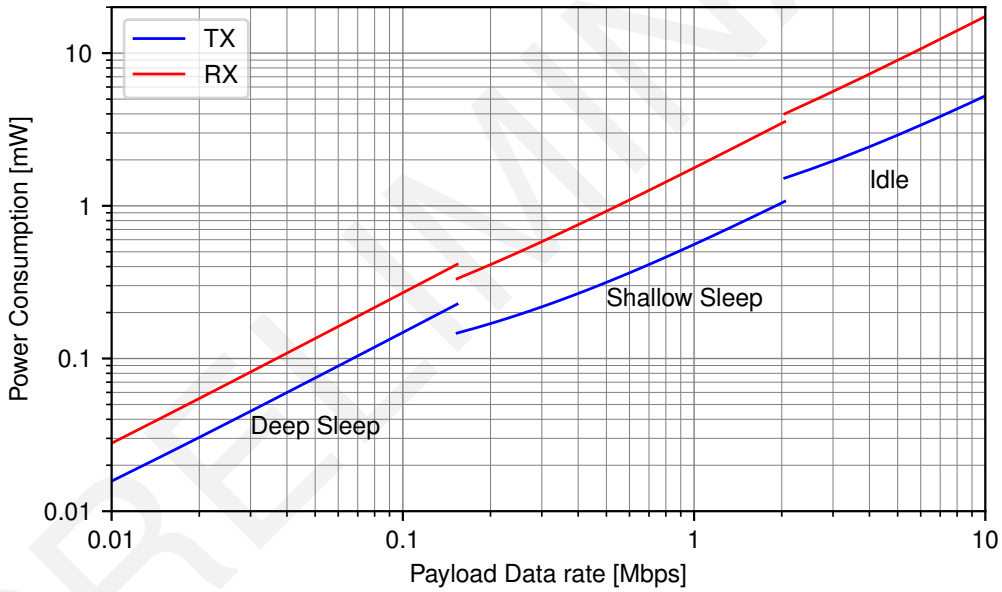


Figure 8: Power consumption, 1.8 V supply, 64 byte packet, FEC 1.33.

6.5 Link Budget

Two factors dictate the link budget of a wireless system: the transmitted energy per symbol, and the receiver sensitivity. In UWB systems, the transmitted energy is subject to limits in both average power and peak power.

The limit on average power during a 1 ms observation time is a power density of -41.3 dBm/MHz. The maximum allowable average power P_{AVG} is given by:

$$P_{AVG} = -41.3 \text{ dBm/MHz} + 10 \cdot \log_{10}(BW_{TX}) - 1 \text{ dB} \quad (2)$$

[8] Includes energy lost in DC-DC capacitor, C_{DCDC} = 360 nF

where BW_{TX} is the used bandwidth during transmission, and a 1 dB margin to the limit is maintained. Occupying a larger transmitter bandwidth will therefore allow a larger energy per symbol.

The energy that can be transmitted in each symbol depends on the achieved data rate as:

$$E_{TX} = P_{AVG} + 10 \cdot \log_{10}\left(\frac{20.48\ \text{MHz}}{DR}\right) + 3\ \text{dB} \tag{3}$$

where DR is the data rate, and the 3 dB is due to the PHY layer sending a maximum of 50% 1s in OOK modulation. The data rate is equal to the number of bits in each packet N_{bits} multiplied by the packet rate R_{packet}.

On the other hand, regulations also place a limit of 0 dBm on the emitted peak power in 50 MHz RBW. This limits the maximum amount of energy in a symbol, regardless of data rate. In practice, at a symbol rate of 20.48 Mbps the maximum E_{TX} is limited to 2 dBm/20 MHz[9].

For high data rates the transmitted energy is therefore limited by the average power requirement, while for low data rate it is limited by the peak power requirement.

At the receiver, the sensitivity at the antenna is:

$$E_{min} = E_{RX,min} - G_R \tag{4}$$

where $E_{RX,min}$ is the receiver sensitivity and G_R is the antenna gain including PCB losses.

The link budget is then given by:

$$\text{Link Budget} = E_{TX} - E_{min} \tag{5}$$

Figure 9 illustrates the link budget for 0 dBi antenna gain and several transmit bandwidths.

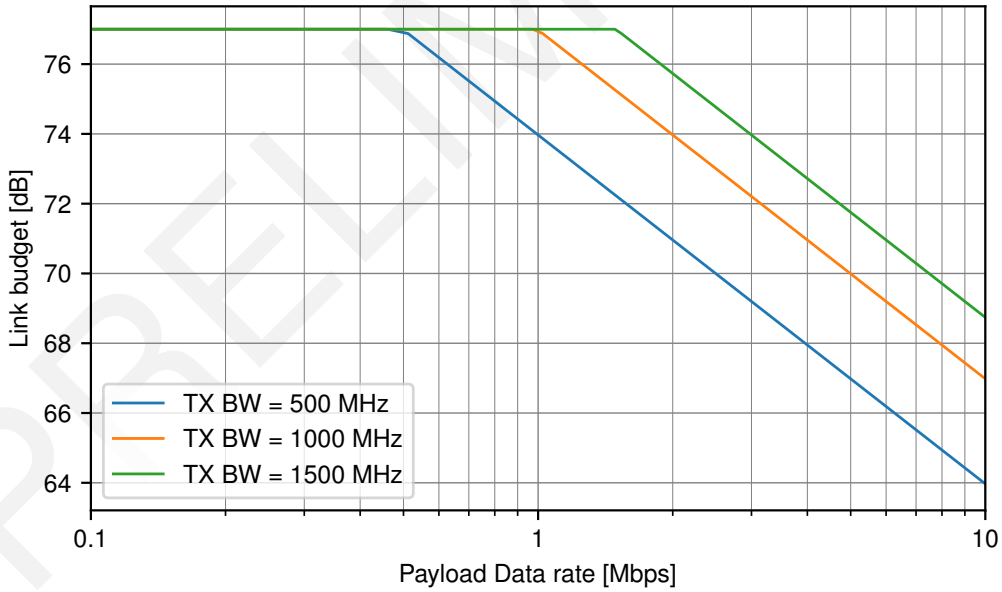


Figure 9: Link budget for 0 dBi antenna gain, FEC 1.33 and 64 Bytes per packet.

[9] An energy of 0 dBm/20 MHz signifies that the average power during a symbol of duration 1/20.48 MHz is 0 dBm, such that if a continuous stream of bit 1 symbols is transmitted the average power is 0 dBm.

6.6 SPI Protocol

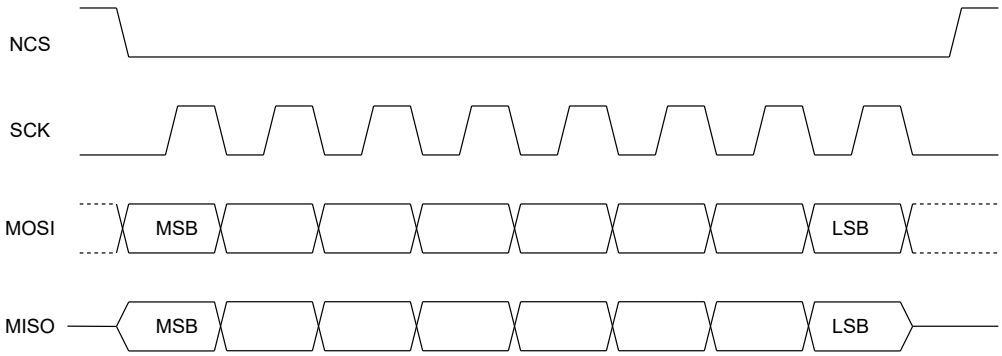


Figure 10: Timing of a single byte on the SPI protocol.

Figure 10 illustrates the timing of the SPI protocol. The CSN pin has to be pulled low during each transaction, the MISO pin is high-Z otherwise. The SPI clock on SCK idles low, MOSI and MISO change on the falling edge of SCK, and are sampled on the rising edge of SCK. The word size of the protocol is a single byte, the MSB is shifted in first, the LSB is shifted in last.

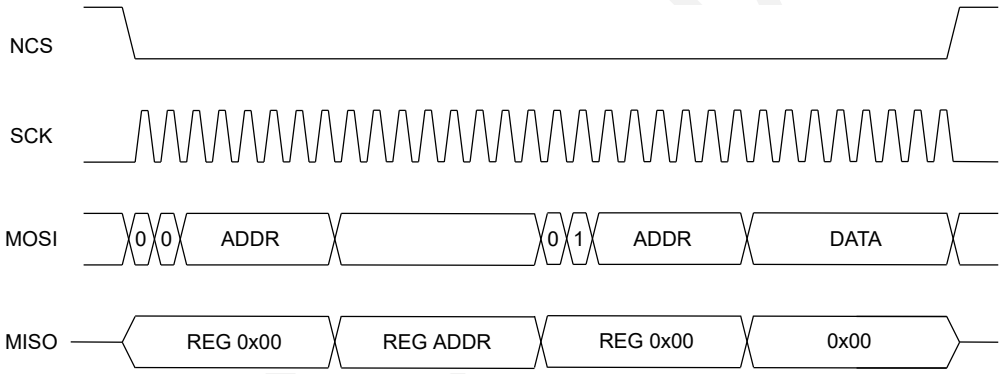


Figure 11: SPI read and write register transaction.

The non-burst read and write register protocol is illustrated in Figure 11. Each read of write starts with a command byte, where the MSB bit indicates if a normal (low bit) or a burst (high bit) transmission is coming, and the MSB-1 bit indicates if the transaction will be read (low bit) or write (high bit), and includes a 6-bit register address. The MISO line will return the contents of the 0x00 register during the command byte.

During a read transaction, the contents of the register indicated by the address in the command byte is returned on MISO, and the second byte on MOSI is ignored.

During a write transaction, the new content of the register indicated by the address in the command byte is put on MOSI, and the second byte on MISO is always 0x00.

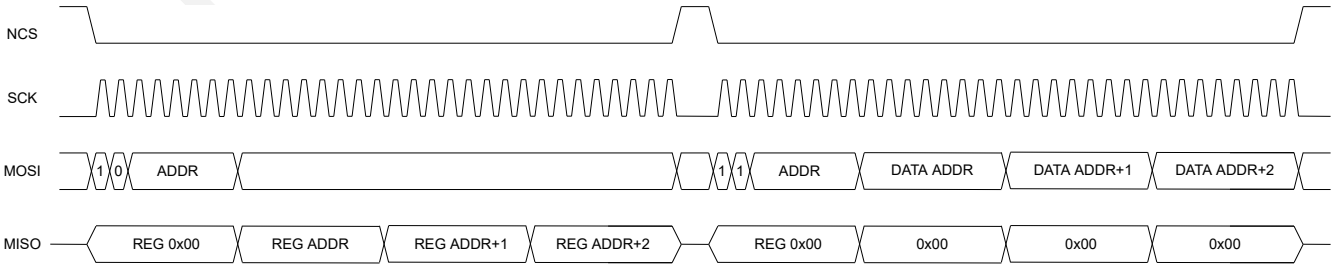


Figure 12: SPI burst read and write transaction.

The burst read and write register protocol is illustrated in Figure 12. To enable burst mode, the MSB bit in the command byte is set high, followed by the read/write flag and the 6-bit address. Subsequent bytes are read from or written to subsequent register addresses, with the address clamped to 0x3F. To exit burst mode, CSN has to be pulled high to end the transaction.

Burst mode allows to read or write a block of registers, or to read or write multiple bytes to the FIFOs (which reside on address 0x3F).

7 PHY Layer

This section outlines the SR1000 series UWB PHY layer with 20.48 MHz symbol rate.

7.1 General

The PHY layer is based on impulse radio signaling in the 6.0 - 9.3 GHz frequency band.

Each radio is free to fill this spectrum, as long as local UWB spectral regulations are met. The aim is to transmit at a fast rate, then release the channel as soon as possible to enhance multi-user co-existence. This type of bursty transmission also greatly reduces power consumption as compared to time-spread UWB standards.

The instantaneous bandwidth of the channel is 500 MHz to facilitate sufficient sensitivity at the receiver. The radio can transmit multiple packets at different RF frequencies in a 1 ms time frame, in order to fill more spectrum and increase the energy in a symbol. Information is encoded in the existence or non existence of a pulse train.

On-Off Keying (OOK) is supported, at a 20.48 MHz symbol rate. The preamble consists of a variable length alternate 1s and 0s, followed by a 32-bit sync word, variable payload, and 16-bit Cyclic Redundancy Check (CRC). The payload and CRC are optionally encoded with a 1/1.33, 1/1.66, or 1/2.0 Viterbi rate, punctured convolutional Forward Error Correction (FEC) code.

7.2 Symbol Structure

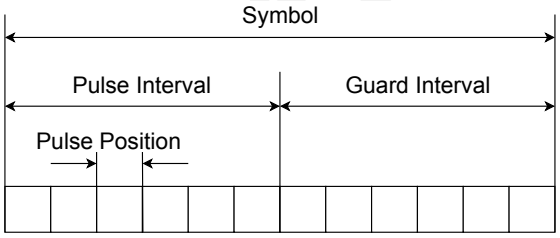


Figure 13: Symbol structure

Figure 13 outlines the structure of a symbol. Each symbol has a length of 1/20.48 MHz, and is subdivided in to 12 pulse positions (of approx. 4 ns length). Each of the first 6 pulse positions can contain a pulse, while the last 6 pulse positions are reserved as a guard interval against Inter Symbol Interference (ISI). A pulse is allowed to spill over in the next pulse position, to support accurate pulse shaping. The radio is free to assign a number of 1 up to 6 pulses of different pulse width and center frequencies to the first 6 pulse positions.

7.3 Encoding

Base

Data	0	1
Symbol	0	1

1-bit Differential

Data	0	1
Symbols	10	01

2-bit Differential

Data	00	01	10	11
Symbols	1000	0100	0010	0001

Figure 14: Encoding formats

Figure 13 outlines the available encoding formats. In the base modulation, the total absence of pulses encoding a 0 bit, and the existence of pulses encodes a 1 bit. Both preamble and sync word shall be encoded by the base modulation only.

In addition, the payload and CRC can be optionally encoded in a half rate 1-bit or 2-bit differential encoding. 1-bit differential encoding represents bits in two OOK modulated symbols, with a zero bit encoded as a 1 followed by a 0, and a one bit encoded as a 0 followed by a 1. 2-bit differential encoding represents two bits in four OOK modulated symbol, one of which carries a 1 symbol and the other 3 carry a 0 symbol.

7.4 Packet Structure

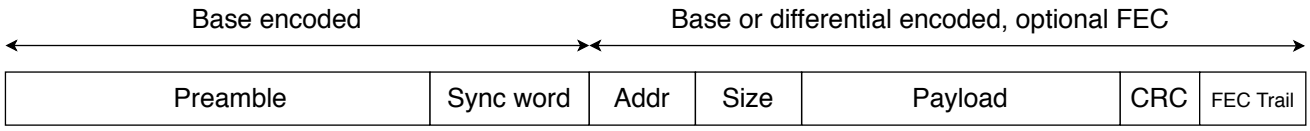


Figure 15: Packet structure

Figure 15 outlines the structure of a packet. Each packet consists of a preamble, sync word, payload and CRC, with optional Address, Size and FEC Trail bits. The optional bits are inserted into the packet structure and do not consume any bits of the Payload.

The preamble is an alternate sequence of 1 and 0 symbols. It is followed by a 32-bit sync word, which is programmable by the MAC layer. The payload has a variable length of 1 up to 128 bytes, followed by a 16-bit CRC calculated over the payload. The CRC polynomial is programmable by the MAC layer.

The default broadcast sync word shall be 0x5EA6C11D. The default broadcast CRC polynomial shall be 0x8005.

Optionally, the PHY layer can append an 8-or 16-bit bit address field and/or 8-bit packet size field at the start of the payload, which is encoded in the same manner.

If the address field is enabled, packet filtering shall be performed in the PHY layer based on the received address. If the packet size field is enabled, the receiver will put that exact amount of bytes into the FIFO, or a maximum number of bytes as indicated by the MAC layer. In default broadcast, these fields shall be disabled and the default packet size shall be 16 bytes.

7.5 Signal Quality and Clear Channel Assesment

The PHY layer shall provide a readout of channel energy called Received Noise Strength Indicator (RNSI), and a readout of symbol energy after sync word triggering called Received Signal Strength Indicator (RSSI).

Access to the channel can optionally be restricted by a Clear Channel Assessment (CCA) check of the channel energy, with adjustable threshold.

7.6 Auto Reply

The PHY layer shall support conditional automatic transmission of a packet after successful packet reception without intervention of the MAC layer. This mechanism facilitates fast and efficient acknowledgment of received packets, as well as a information return channel. The Auto Reply packet payload shall be loaded into the transmit FIFO before primary reception occurs.

8 Registers

8.1 Overview

Table 18: Register Overview

Address	Read	Write
0x00	Status bits 1	Interrupt mask 1
0x01	Status bits 2	Interrupt mask 2
0x02	TX buffer load	TX buffer threshold
0x03	RX buffer load	RX buffer threshold
0x04	Sleep config	
0x05	Timer config	
0x06	Timer count MSB	Timer period MSB
0x07	Timer count LSB	Timer period LSB
0x08	RX timeout	
0x09	RX timeout + RX powerup time	
0x0A	Power up delay	
0x0B	Reserved	
0x0C	Reserved	
0x0D	Baseband tuning	
0x0E	Peripheral controls	
0x0F	RX tuning	
0x10	TX pulse 12	
0x11	TX pulse 11	
0x12	TX pulse 10	
0x13	TX pulse 9	
0x14	TX pulse 8	
0x15	TX pulse 7	
0x16	TX pulse 6	
0x17	TX pulse 5	
0x18	TX pulse 4	
0x19	TX pulse 3	
0x1A	TX pulse 2	
0x1B	TX pulse 1	
0x1C	Pulse parameters	
0x1D	Baseband tuning	
0x1E	Calibration result	Calibration code
0x1F	Power status	Main Commands
0x20	NVM value	NVM inputs
0x21	Reserved	
0x22	RSSI	
0x23	RNSI	
0x24	RX waiting time MSB	RX waiting time selection
0x25	RX waiting time LSB	
0x26	Received address MSB	

0x27	Received address LSB	
0x28	Reserved	
0x29	Reserved	
0x2A	Reserved	
0x2B	Reserved	
0x2C	Main modem features	
0x2D	Reserved	
0x2E	Reserved	
0x2F	Preamble length	
0x30	Constant gains	
0x31	Reserved	
0x32	Sync word's 1st byte	
0x33	Sync word's 2nd byte	
0x34	Sync word's 3rd byte	
0x35	Sync word's 4th byte	
0x36	CRC polynomal MSB	
0x37	CRC polynomal LSB	
0x38	TX address MSB	
0x39	TX address LSB	
0x3A	RX address MSB	
0x3B	RX address LSB	
0x3C	TX packet size	
0x3D	RX packet size	
0x3E	Packet config	
0x3F	RX FIFO output	TX FIFO input

8.2 Register 0x00: Main device flags

Table 20: Register 0x00

bit	7	6	5	4	3	2	1	0
read	STAT2IRQ	PKBEGINI	RXTIMEOI	TXENDI	NEWPKTI	ADDRMATI	BRDCASTI	CRCPASSI
write	IRQPOLAR	PKBEGINE	RXTIMEOE	TXENDE	NEWPKTE	ADDRMATE	BRDCASTE	CRCPASSE
default	1	0	0	1	1	0	0	0

STAT2IRQ = Auxiliary Device Flags Status: 1 if any IRQ flag is set in register 0x01, 0 otherwise.

PKBEGINI = Packet beginning interrupt: set when transmitter or receiver reaches synchronization word, cleared on read.

RXTIMEOI = Receiver timeout interrupt: set when receiver times out on a packet, cleared on read.

TXENDI = Packet transmission end interrupt: set when transmitter completes packet transmission, cleared on read.

NEWPKTI = New packet reception interrupt: set when receiver completes packet reception, cleared on read.

ADDRMATI = New packet address field match interrupt: set when receiver matches the address field, cleared on read.

BRDCASTI = New broadcast packet reception end interrupt: set when receiver matches a broadcast address (all ones), cleared on read.

CRCPASSI = New packet CRC pass interrupt: set when receiver matches valid CRC field, cleared on read.

IRQPOLAR = Interrupt ReQuest output pin polarity: 1 the IRQ pin is active high, 0 the IRQ pin is active low.

PKBEGINE = Packet beginning interrupt enable: 1 PKBEGINI interrupt will assert IRQ pin, 0 no effect.

RXTIMEOE = Receiver timeout interrupt enable: 1 RXTIMEOI interrupt will assert IRQ pin, 0 no effect.

TXENDE = Packet transmission end interrupt enable: 1 TXENDI interrupt will assert IRQ pin, 0 no effect.

NEWPKTE = New packet reception interrupt enable: 1 NEWPKTI interrupt will assert IRQ pin, 0 no effect.

ADDRMATE = New packet address field match interrupt enable: 1 ADDRMATI interrupt will assert IRQ pin, 0 no effect.

BRDCASTE = New broadcast packet reception end interrupt enable: 1 BRDCASTI interrupt will assert IRQ pin, 0 no effect.

CRCPASSE = New packet CRC pass interrupt enable: 1 CRCPASSI interrupt will assert IRQ pin, 0 no effect.

8.3 Register 0x01: Auxiliary device flags

Table 21: Register 0x01

bit	7	6	5	4	3	2	1	0
read	XOTIMERI	WAKEUPI	CSCFAILI	TXUDRFLI	RXOVRFLI	TXOVRFLI	BUFLOADI	BUFSTOPI
write	XOTIMERE	WAKEUPE	CSCFAILE	TXUDRFLE	RXOVRFLE	TXOVRFLE	BUFLOADE	BUFSTOPE
default	0	1	1	1	1	1	1	0

XOTIMERI = Crystal oscillator timer interrupt: set when crystal timer reaches zero, cleared on read.

WAKEUPI = Wake-up interrupt: set when radio finishes waking up, cleared on read.

CSCFAILI = Carrier sensing check failure interrupt: set when receiver senses carrier over threshold, cleared on read.

TXUDRFLI = Transmission buffer underflow interrupt: set when transmitter attempts read on empty TX FIFO, cleared on read.

RXOVRFLI = Reception buffer overflow interrupt: set when receiver attempts write on full RX FIFO, cleared after FLUSHRX command.

TXOVRFLI = Transmission buffer overflow interrupt: set when SPI attempts write on full TX FIFO, cleared after FLUSHTX command.

BUFLOADI = Data buffer load threshold interrupt: set when currently used FIFO (RX if RXMODE = 1, TX otherwise) is below its threshold (RXTHRESH if RXMODE = 1, TXTHRESH otherwise), cleared otherwise.

BUFSTOPI = Data buffer stop interrupt: set when either the RX FIFO has less than two bytes (if RXMODE = 1), or the TX FIFO has less than two bytes of free space left (if RXMODE = 0). Cleared otherwise.

XOTIMERE = Crystal oscillator timer interrupt enable: 1 XOTIMERI interrupt will assert IRQ pin, 0 no effect.

WAKEUPE = Wake-up interrupt enable: 1 WAKEUPI interrupt will assert IRQ pin, 0 no effect.

CSCFAILE = Carrier sensing check failure interrupt enable: 1 CSCFAILI interrupt will assert IRQ pin, 0 no effect.

TXUDRFLE = Transmission buffer underflow interrupt enable: 1 TXUDRFLI interrupt will assert IRQ pin, 0 no effect.

RXOVRFLE = Reception buffer overflow interrupt enable: 1 RXOVRFLI interrupt will assert IRQ pin, 0 no effect.

TXOVRFLE = Transmission buffer overflow interrupt enable: 1 TXOVRFLI interrupt will assert IRQ pin, 0 no effect.

BUFLOADE = Data buffer load threshold interrupt enable: 1 BUFLOADI interrupt will assert IRQ pin, 0 no effect.

BUFSTOPE = Data buffer load stop interrupt enable: 1 BUFSTOPI interrupt will assert IRQ pin, 0 no effect.

8.4 Register 0x02: Transmission buffer status

Table 22: Register 0x02

bit	7	6	5	4	3	2	1	0
read	TXBUFLOAD							
write	TXIRQEN	TXTHRESH						
default	0	0b0000000						

TXBUFLOAD = Transmission buffer load: number of bytes of data in TX FIFO.

TXIRQEN = Transmission buffer load threshold enable: when set, BUFLOADI will be affected by the transmitter buffer load threshold.

TXTHRESH = Transmission buffer load threshold: number of bytes in TX FIFO below which BUFLOADI can be triggered.

8.5 Register 0x03: Reception buffer status

Table 23: Register 0x03

bit	7	6	5	4	3	2	1	0
read	RXBUFLOAD							
write	RXIRQEN	RXTHRESH						
default	0	0b0000000						

RXBUFLOAD = Receiver buffer load: number of bytes of data in RX FIFO.

RXIRQEN = Receiver buffer load threshold enable: when set, BUFLOADI will be affected by the receiver buffer load threshold.

RXTHRESH = Receiver buffer load threshold: number of bytes in RX FIFO above which BUFLOADI can be triggered.

8.6 Register 0x04: Sleep configuration

Table 24: Register 0x04

bit	7	6	5	4	3	2	1	0
r/w	SLPDEPTH		SLPRXTO	SLPTXEND	SLPRXEND	SLPMATCH	SLPBRDCA	SLPNOISY
default	0b11		0	0	0	0	0	0

SLPDEPTH = Sleeping depth level: sleep level that will be entered after sleep is triggered. 0b00 or 0b10 idle, 0b01 shallow sleep, 0b11 deep sleep.

SLPRXTO = Sleep on receiver timeout event: if set, sleep will be triggered by a receiver timeout event in RX-TIMEOI.

SLPTXEND = Sleep on packet transmission end event: if set, sleep will be triggered by a packet transmission end event in TXENDI.

SLPRXEND = Sleep on new packet reception end event: if set, sleep will be triggered by a new packet reception end event in NEWPKTI.

SLPMATCH = Sleep on new packet address field match event: if set, sleep will be triggered by a new packet address field match event in ADDRMATI.

SLPBRDCA = Sleep on new broadcast packet reception end event: if set, sleep will be triggered by a new broadcast packet reception end event in BRDCASTI.

SLPNOISY = Sleep on carrier sensing check failure event: if set, sleep will be triggered by a carrier sensing check failure event in CSCFAILI.

8.7 Register 0x05: Timer configuration

Table 25: Register 0x05

bit	7	6	5	4	3	2	1	0
r/w	AUTOWAKE	WAKEONCE	SYNATEND	SYNTXBEG	SYNRXBEG	SYNMATCH	SYNBRDCA	SYNRXCRC
default	0	0	0	0	0	0	0	0

AUTOWAKE = Automatically wake-up the device from sleep: if set, wake up from sleep will happen when the wake-up timer triggers.

WAKEONCE = Wake-up automatically only once from sleep timer: if set, automatic wake up from sleep can occur only once until SLPPERIOD is overwritten.

SYNATEND = Synchronize wake-up timer at the end of packets: 1 SYNPKTTX and SYNPKTRX observe beginning of packets, 0 SYNPKTTX and SYNPKTRX observe endings of packets.

SYNPKTTX = Synchronize wake-up timer on packet transmission event: if set, wake up timer is reset at either transmission of sync word (SYNATEND = 0) or after finishing packet transmission (SYNATEND = 1).

SYNPKTRX = Synchronize wake-up timer on packet reception event: if set, wake up timer is reset at either reception of sync word (SYNATEND = 0) or after finishing packet reception (SYNATEND = 1).

SYNMATCH = Synchronize wake-up timer on received packet address field match event: if set, wake up timer is reset if the packet address field matches the receiver's own address. If SYNRXCRC is set, both conditions have to be met to trigger a reset.

SYNBRDCA = Synchronize wake-up timer on received broadcast packet address field match event: if set, wake up timer is reset at the end of reception of a packet with a matching sub-network broadcast address. If SYNRXCRC is set, both conditions have to be met to trigger a reset.

SYNRXCRC = Synchronize wake-up timer on CRC pass event: if set, a wake up timer reset requires a correct CRC field upon reception.

8.8 Register 0x06 - 0x07: Timer counter

Table 26: Register 0x06

bit	7	6	5	4	3	2	1	0
read	XTALCOUNT8							
write	SLPPERIOD8							
default	0x08							

Table 27: Register 0x07

bit	7	6	5	4	3	2	1	0
read	XTALCOUNT0							
write	SLPPERIOD0							
default	0x00							

XTALCOUNT = Crystal oscillator clock wake-up timer count: returns current XTAL timer count value, regardless of sleep level.

SLPPERIOD = Wake-sleep (power-cycling) period in number of clock cycles: value at which the wake up timer resets to 0x0000 and potentially trigger an automatic wake up. The actual power-cycling period duration depends on the sleep level selected in register field SLPDEPTH at register address 0x04. It will use either the PLL clock of 20.48 MHz (when sleep depth is set to idle), or the crystal clock of 32.768 kHz (when sleep depth is shallow or deep sleep).

8.9 Register 0x08 - 0x09: Receiver timeout and power-up delay

Table 28: Register 0x08

bit	7	6	5	4	3	2	1	0
r/w	RXPERIOD4							
default	0xFF							

Table 29: Register 0x09

bit	7	6	5	4	3	2	1	0
r/w	RXPERIOD0				RXPUDELAY			
default	0xF				0x3			

RXPERIOD = Receiver timeout period: receiver will wait RXPERIOD*8+1 symbol clock cycles to detect a packet before raising the timeout flag.

RXPUDELAY = Receiver power-up delay: receiver will wait RXPUDELAY+1 symbol clock cycles to settle before attempting packet reception.

8.10 Register 0x0A: Transceiver power-up delay

Table 30: Register 0x0A

bit	7	6	5	4	3	2	1	0
r/w	PWRUPDEL							
default	0x00							

PWRUPDEL = Fine-grained transceiver power-up delay: after wake-up, modem will wait 4*PWRUPDEL symbol clock cycles in idle sleep mode before powering up the transmitter or receiver.

8.11 Register 0x0B: Reserved

Table 31: Register 0x0B

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.12 Register 0x0C: Reserved

Table 32: Register 0x0C

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.13 Register 0x0D: Calibration

Table 33: Register Address 0x0D

bit	7	6	5	4	3	2	1	0
r/w	LNAIMPED	PLL_RES			VREF_TUNE			
default	0	0b010			0b1010			

This register holds the calibration values. During the manufacturing process, calibration information is stored as a byte in the non-volatile memory (NVM).

LNAIMPED = Reserved.

PLL_RES = Phase-locked loop voltage-controlled oscillator resistor tuning.

VREF_TUNE = Transceiver supply voltage reference tuning.

8.14 Register 0x0E: Disables and clock control

Table 34: Register 0x0E

bit	7	6	5	4	3	2	1	0
r/w	STDSPI	FLUSHDIS	1VSW_DIS	DCDC_DIS	PLL_DIS	SYMBCSRC	XTALCSRC	OUTPXTAL
default	1	0	0	0	0	0	0	0

STDSPI = Standard SPI operation: 1 MISO changes on falling edge of SCK, 0 MISO changes on rising edge of SCK.

FLUSHDIS = Reception buffer auto-flush disable bit:

0 = this is the default behavior. The RX FIFO is filled, but it will get flushed automatically upon reception of a faulty or rejected packet.

1 = the automatic flush feature is disabled.

It is strongly advised to wait for the end of the frame reception or, if it's not an option (i.e for for payload sizes beyond 128 bytes), to disable this feature.

1VSW_DIS = Storage capacitor switch disable bit: 1 disable, 0 enable power gating of 1V internal supply.

DCDC_DIS = DC-DC converter disable bit: 1 disable, 0 enable internal DC-DC converter.

PLL_DIS = PLL disable bit: 1 disable, 0 enable internal PLL.

SYMBCSRC = Symbol rate clock source: 1 clock on PLL_CLK pin is used for symbol clock, 0 internal PLL is used for symbol clock.

Warning: As SYMBCSRC = 0 by default at reset, if an external oscillator is connected to PLL_CLK pin and if the same oscillator is also used as the main clock of an other integrated circuit, it will be pulled down to ground at reset, which might prevent this other integrated circuit to reset properly.

XTALCSRC = Crystal oscillator clock source: 1 clock on XTAL_CLK is used for crystal clock, 0 internal XTAL is used for crystal clock.

Warning: As XTALCSRC = 0 by default at reset, if an external oscillator is connected to XTAL_CLK pin and if the same oscillator is also used as the main clock of an other integrated circuit, it will be pulled down to ground at reset, which might prevent this other integrated circuit to reset properly.

OUTPXTAL = Output crystal oscillator clock: if set, internal crystal clock is output on XTAL_CLK pin.

8.15 Register 0x0F: Receiver frequency tuning

Table 35: Register Address 0x0F

bit	7	6	5	4	3	2	1	0
r/w	LNA_PEAK			RFFILFREQ				
default	0b110			0b01010				

This register configures the receiver for optimal reception for a given center frequency.

LNAPEAK = Low-noise amplifier peak frequency.

RFFILFREQ = Radio-frequency filter frequency. This register field sets the center frequency of the receiver's radio-frequency active pass-band.

8.16 Register 0x10 - 0x1B: Transmitted pulse pattern

Table 36: Register Address 0x10

bit	7	6	5	4	3	2	1	0
r/w	PULSE12WID			PULS12FREQ				
default	0b000			0b00000				

Table 37: Register Address 0x11

bit	7	6	5	4	3	2	1	0
r/w	PULSE11WID			PULS11FREQ				
default	0b110			0b10100				

Table 38: Register Address 0x12

bit	7	6	5	4	3	2	1	0
r/w	PULSE10WID			PULS10FREQ				
default	0b110			0b10110				

Table 39: Register Address 0x13

bit	7	6	5	4	3	2	1	0
r/w	PULSE9WID			PULS9FREQ				
default	0b110			0b11000				

Table 40: Register Address 0x14

bit	7	6	5	4	3	2	1	0
r/w	PULSE8WID			PULS8FREQ				
default	0b110			0b11010				

Table 41: Register Address 0x15

bit	7	6	5	4	3	2	1	0
r/w	PULSE7WID			PULS7FREQ				
default	0b000			0b00000				

Table 42: Register Address 0x16

bit	7	6	5	4	3	2	1	0
r/w	PULSE6WID			PULS6FREQ				
default	0b000			0b00000				

Table 43: Register Address 0x17

bit	7	6	5	4	3	2	1	0
r/w	PULSE5WID			PULS5FREQ				
default	0b000			0b00000				

Table 44: Register Address 0x18

bit	7	6	5	4	3	2	1	0
r/w	PULSE4WID			PULS4FREQ				
default	0b000			0b00000				

Table 45: Register Address 0x19

bit	7	6	5	4	3	2	1	0
r/w	PULSE3WID			PULS3FREQ				
default	0b000			0b00000				

Table 46: Register Address 0x1A

bit	7	6	5	4	3	2	1	0
r/w	PULSE2WID			PULS2FREQ				
default	0b000			0b00000				

Table 47: Register Address 0x1B

bit	7	6	5	4	3	2	1	0
r/w	PULSE1WID			PULS1FREQ				
default	0b000			0b00000				

These registers configure the pulses to be generated within a symbol. Refer to the PHY Layer section for an outline of the structure of a symbol. Pulse at position 12 and 1, configured at register 0x10 and 0x1B respectively, must stay disabled at all time for proper operation since these pulse positions act as guard interval against Inter Symbol Interference (ISI). To disable a pulse, the whole pulse configuration register must be set to 0x00.

PULSEnWID = Width of nth pulse : This register field sets the pulse duration of all pulses at the nth pulse position of each symbol transmitted. A wider pulse translates to more output power. This table shows the pulses duration when the signal is over its 50% magnitude.

Table 48: Pulse Width

3-bit code	Pulse duration
0	0.90 ns
1	1.08 ns
2	1.15 ns
3	1.30 ns
4	1.50 ns
5	1.67 ns
6	1.87 ns
7	2.05 ns

PULSnFREQ = Frequency of pulse n: This register field sets the center frequency of all pulses at the nth pulse position of each symbol transmitted.

8.17 Register 0x1C: Shared pulse parameters

Table 49: Register Address 0x1C

bit	7	6	5	4	3	2	1	0
read	HOLDTXON	RNDPHASE	TX_POWER		IFFILTEN	VDDLEVEL		
write	HOLDTXON	RNDPHASE	TX_POWER		IFFILTEN	-		
default	0	1	0b00		0	-		

HOLDTXON = Reserved.

RNDPHASE = Reserved.

TX_POWER = Transmission power. This register field adjusts the power level of the transmitter by attenuating it. The default value of 0b00 results in the maximum transmission power and a value of 0b11 attenuates it by around 1.8 dB.

IFFILTEN = Reserved.

VDDLEVEL = Reserved.

8.18 Register 0x1D: Baseband tuning

Table 50: Register Address 0x1D

bit	7	6	5	4	3	2	1	0
read	DL_TUNE				LEAD_LAG	INTEGLEN	INTEGGAIN	
write	DL_TUNE				CAGAINOV	INTEGLEN	INTEGGAIN	
default	0b1000				0	0	0b01	

This register adjusts the timing of the transmitted pulse positions.

DL_TUNE = Delay line tuning value.

LEAD_LAG = Delay line leads or lag the symbol rate.

CAGAINOV = Reserved.

INTEGLEN = Reserved.

INTEGGAIN = Reserved.

8.19 Register 0x1E: DCRO calibration

Table 51: Register Address 0x1E

bit	7	6	5	4	3	2	1	0
read	DCRO_FREQ							
write	-			DCRO_CODE				
default	-			0b01010				

This register is used during frequency calibration to obtain the exact center frequency in MHz corresponding to one of the 32 available frequency codes.

DCRO_FREQ = Center frequency. This register field contains the frequency expressed in multiples of 41 MHz corresponding to the 5-bit frequency code held in register field DCRO_CODE.

DCRO_CODE = Frequency code. This write-only register field provides the 5-bit frequency code for which the on-chip calibration block will measure the corresponding center frequency.

8.20 Register 0x1F: Power status and commands

Table 52: Register 0x1F

bit	7	6	5	4	3	2	1	0
read	NVM_EN	RX_EN	TX_EN	AWAKE	MODEM_ON	DCDC_EN	PLL_EN	REF_EN
write	Reserved	SKIPWAKE	RXMODE	STARTTX	INITIMER	GOTOSLP	FLUSHRX	FLUSHTX
default	0	0	1	0	0	0	0	0

NVM_EN = NVM enabled: returns 1 if the NVM is powered up, 0 otherwise.

RX_EN = Receiver enabled: returns 1 if the receiver is powered up, 0 otherwise.

TX_EN = Transmitter enabled: returns 1 if the transmitter is powered up, 0 otherwise.

AWAKE = Device is completely awake: returns 1 if awake and not in sleep, 0 otherwise.

MODEM_ON = Modem is on: returns 1 if the modem is powered up and in a ready state, 0 otherwise.

DCDC_EN = DC-DC converter enabled: returns 1 if the DC-DC converter is enabled, 0 otherwise.

PLL_EN = PLL enabled: returns 1 if the PLL is powered up, 0 otherwise.

REF_EN = Reference buffers enabled: returns 1 if the buffers are enabled, 0 otherwise.

SKIPWAKE = Skip next scheduled wake-up: writing a 1 will skip the next wake-up trigger.

RXMODE = Receiver mode device operation: 1 receiver mode, 0 transmitter mode. When this register bit is set to '1', the whole device is configured for frame reception and the modem powers up the receiver expecting a frame whenever it is not asleep or powered down. When this register bit is set to '0', the whole device is configured for frame transmissions and will respond to frame transmission requests set by writing a '1' into the register bit START_TX as long as it is not asleep.

STARTTX = Start transmission: writing a 1 will schedule packet transmission at the next available moment.

INITIMER = Initialize wake-up timers: writing a 1 will reset the wake up timers.

GOTOSLP = Go to sleep: writing a 1 will schedule going to sleep after the modem is not busy sending or receiving a packet. Writing a 0 will wake up the device if AUTOWAKE = 0.

FLUSHRX = Flush and reset reception buffer: writing a 1 will empty the RX FIFO and reset its overflow flag.

FLUSHTX = Flush and reset transmission buffer: writing a 1 will empty the TX FIFO and reset its overflow flag.

8.21 Register 0x20: NVM

Table 53: Register 0x20

bit	7	6	5	4	3	2	1	0
read	ROM_BYTE							
write	ROMPWRSW	ROM_ADDR						

ROM_BYTE = NVM output byte: returns current output byte of NVM.

ROMPWRSW = NVM power switch: 1 enable, 0 disable NVM

ROM_ADDR = NVM byte address: sets current address to be read on NVM

8.22 Register 0x21: Reserved

8.23 Register 0x22: Receiver last RSSI

Table 54: Register 0x22

bit	7	6	5	4	3	2	1	0
read	0b00		RSSI					

RSSI = Received Signal Strength Indicator: returns RSSI indicator for last received packet. Its value is representative of the actual signal strength of the last frame received only if the receiver gain is adjusted automatically by the modem.

8.24 Register 0x23: Receiver last RNSI

Table 55: Register 0x23

bit	7	6	5	4	3	2	1	0
read	0b00		RNSI					

RNSI = Received Noise Strength Indicator: returns last valid RNSI indicator. Its value is representative of the background noise level captured by the receiver only if the receiver's gain is adjusted automatically by the modem.

8.25 Register 0x24 - 0x25: Receiver last waited time

Table 56: Register 0x24

bit	7	6	5	4	3	2	1	0
read	Reserved	RX_WAITED8						
write	Reserved	-						

Table 57: Register 0x25

bit	7	6	5	4	3	2	1	0
read	RX_WAITED0							
write	-							

RX_WAITED = Receiver time waited: returns number of symbol clock periods counted by the modem while waiting in reception mode for information to decode before detecting the last received frame's synchronization word.

8.26 Register 0x26 - 0x27: Last address received

Table 58: Register 0x26

bit	7	6	5	4	3	2	1	0
read	FRAMEADDR8							

Table 59: Register 0x27

bit	7	6	5	4	3	2	1	0
read	FRAMEADDR0							

FRAMEADDR = Last received frame address field value: returns last address field from a received packet. Only the lower byte (address 0x27) is used when using 8-bit addressing.

8.27 Register 0x28: Reserved

Table 60: Register 0x28

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.28 Register 0x29: Reserved

Table 61: Register 0x29

bit	7	6	5	4	3	2	1	0
read	Reserved							

8.29 Register 0x2A: Reserved

Table 62: Register 0x2A

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.30 Register 0x2B: Reserved

Table 63: Register 0x2B

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.31 Register 0x2C: Modem main features

Table 64: Register 0x2C

bit	7	6	5	4	3	2	1	0
r/w	AUTOTX	AUTORPLY	Reserved		MODCODE		FECLEVEL	
default	0	0	0b00		0b00		0b00	

AUTOTX = Automatic transmission: if set, the modem will attempt transmission after waking up from sleep.

AUTORPLY = Automatic frame reply enable: if set, the modem will switch to transmit a packet after successful packet reception, and vise-versa enter reception mode after successful packet transmission.

MODCODE = Digital Modulation Coding :

If MODCODING = 0b00, the modem uses the 'OOK' modulation coding which simply translates each '0' into a blank symbol (a symbol clock cycle with no pulse emitted) and each '1' into a pulsed symbol (a symbol clock cycle occupied by a pulse bundle).

If MODCODING = 0b01, the modem uses the 'invertible OOK' modulation coding which differs from plain 'OOK' modulation in that the meaning of all symbols over an entire frame can be inverted and a header field is added to the frame to indicate to the receiver of said frame whether all the information contained in it is bit-flipped or not.

FECLEVEL = Forward error correction level:

- 0b00 : no FEC
- 0b01 : FEC rate = 1.33
- 0b10 : FEC rate = 1.66

- 0b11 : FEC rate = 2.00

8.32 Register 0x2D: Reserved

Table 65: Register 0x2D

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.33 Register 0x2E: Reserved

Table 66: Register 0x2E

bit	7	6	5	4	3	2	1	0
r/w	Reserved							

8.34 Register 0x2F: Preamble length

Table 67: Register 0x2F

bit	7	6	5	4	3	2	1	0
r/w	PREAMBLEN							
default	0x27							

PREAMBLEN = Packet preamble length: sets the length of the preamble to (PREAMBLEN+7)*2 symbol clock cycles.

8.35 Register 0x30: Reserved

8.36 Register 0x31: Reserved

8.37 Register 0x32 - 0x35: Sync word

Table 68: Register 0x32

bit	7	6	5	4	3	2	1	0
r/w	SYNCWORD24							
default	0x5E							

Table 69: Register 0x33

bit	7	6	5	4	3	2	1	0
r/w	SYNCWORD16							
default	0xA6							

Table 70: Register 0x34

bit	7	6	5	4	3	2	1	0
r/w	SYNCWORD8							
default	0xC1							

Table 71: Register 0x35

bit	7	6	5	4	3	2	1	0
r/w	SYNCWORD0							
default	0x1D							

SYNCWORD = Synchronization word: 32 bit synchronization word.

8.38 Register 0x36 - 0x37: CRC polynomal

Table 72: Register 0x36

bit	7	6	5	4	3	2	1	0
r/w	CRCPOLYNO8							
default	0x00							

Table 73: Register 0x37

bit	7	6	5	4	3	2	1	0
r/w	CRCPOLYNO0							
default	0x00							

CRCPOLYNO = CRC generator's polynomial: polynomial used to generate CRC check. This CRC feature is not designed to function with empty payloads and thus should be disabled if the payload size is zero.

8.39 Register 0x38 - 0x39: Transmitter address

Table 74: Register 0x38

bit	7	6	5	4	3	2	1	0
r/w	REMOTADDR8							
default	0x00							

Table 75: Register 0x39

bit	7	6	5	4	3	2	1	0
r/w	REMOTADDR0							
default	0x00							

REMOTADDR = Remote node address: address word to put in the packet address field during transmission.

8.40 Register 0x3A - 0x3B: Receiver address

Table 76: Register 0x3A

bit	7	6	5	4	3	2	1	0
r/w	LOCALADDR8							
default	0x00							

Table 77: Register 0x3B

bit	7	6	5	4	3	2	1	0
r/w	LOCALADDR0							
default	0x00							

LOCALADDR = Local node address: address word to compare to for received packets.

8.41 Register 0x3C: Transmitter packet size

Table 78: Register 0x3C

bit	7	6	5	4	3	2	1	0
r/w	TXPKTSIZE							
default	0x10							

TXPKTSIZE = Transmitted packet's payload size: size in bytes of the payload in the next transmitted packet.

8.42 Register 0x3D: Receiver packet size

Table 79: Register 0x3D

bit	7	6	5	4	3	2	1	0
r/w	RXPKTSIZE							
default	0x10							

RXPKTSIZE = Received packet's payload size: size in bytes of the payload in the next received packet.

8.43 Register 0x3E: Packet configuration

Table 80: Register 0x3E

bit	7	6	5	4	3	2	1	0
r/w	ADDRFILT		ADDRLEN	ADDRHDRE	SIZEHDRE	SIZESRC	SAVEADDR	SAVESIZE
r/w	0x00		0	0	0	0	0	0

ADDRFILT = Address field-based hardware packet filtering: 0b00 no filtering, 0b01 reject received packet based on address, 0b10 only auto reply on address match, 0b11 reject packet and cancel autoreply on address mismatch.

ADDRLEN = Address field length: 1 16-bit address field, 0 8-bit address field.

ADDRHDRE = Packet destination address field header enable: 1 enable, 0 disable address field in transmitted packet.

SIZEHDRE = Packet size field header enable: 1 enable, 0 disable size field in transmitted packet.

SIZESRC = Transmission packet payload size source: 1 TXPKTSIZE , 0 first byte in FIFO as source for the transmitted packet size.

SAVEADDR = Save packet address field in reception buffer: 1 packet address will be saved as first bytes in the RX FIFO during packet reception.

SAVESIZE = Save packet payload size field in reception buffer: 1 packet size will be saved as first byte in the RX FIFO during packet reception.

8.44 Register 0x3F: FIFO

Table 81: Register 0x3F

bit	7	6	5	4	3	2	1	0
read	RXBUFFER							
write	TXBUFFER							

RXBUFFER = Receiver's data buffer: reading will extract bytes from the RX FIFO.

TXBUFFER = Transmitter's data buffer: writing will put bytes into the TX FIFO.

9 Package Information

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.65	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	J	2.6	2.7	2.8
EP SIZE Y	K	2.6	2.7	2.8
LEAD LENGTH	L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ccc		0.08	
LEAD OFFSET	ddd		0.1	
EXPOSED PAD OFFSET	eee		0.1	

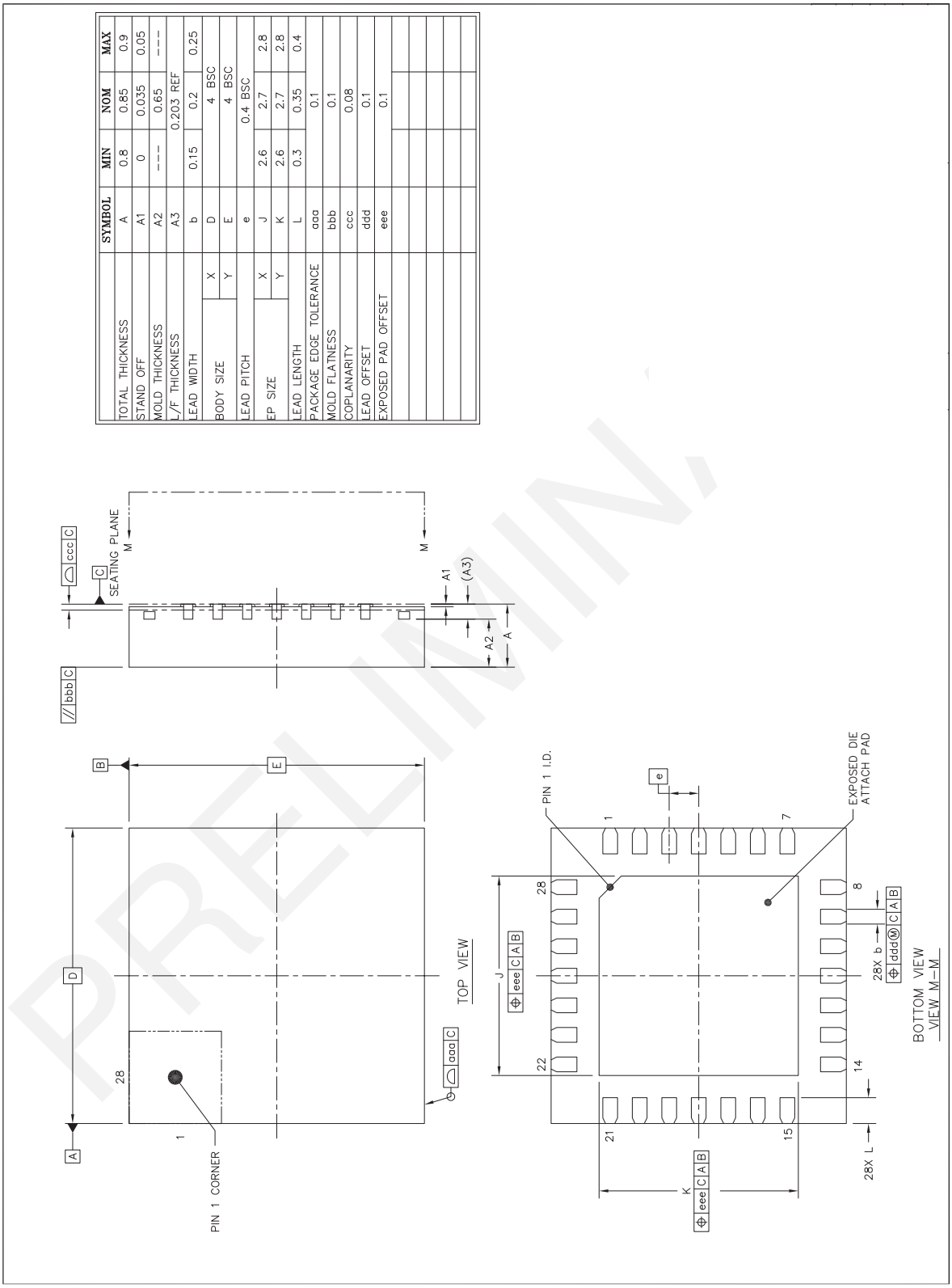
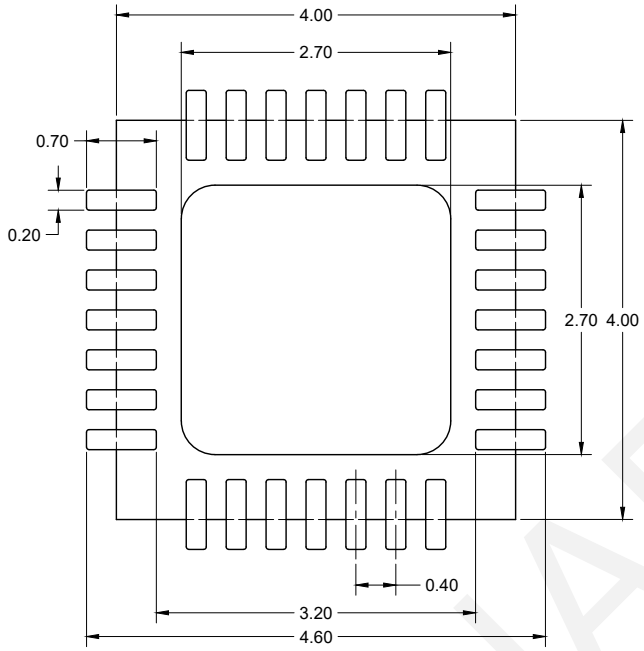


Figure 16: QFN28 package outline drawing



Non solder mask defined pads (NSMD) recommended
Dimensions are in mm

Figure 17: QFN28 recommended footprint

10 Revisions

Table 82: Revisions

REVISION	SECTION	COMMENTS
1.02	1.3	Added device information.
1.01	6.6	Added SPI protocol definition.
1.0		Initial revision.

List of Figures

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